Notice of Allowability	Application No.	Applicant(s)	
	10/767,775	MILLER, KEVIN LEE	
	Examiner	Art Unit	
	Brian Young	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed 1/10/05*.

2. ☒ The allowed claim(s) is/are *1-24*.

3. ☒ The drawings filed on *30 January 2004* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

1. Claims 1-24 are allowed.

2. The following is an examiner's statement of reasons for allowance: a modulator circuit having a mapping function performed within a main feedback loop of the modulator, rather than after the feedback loop, the modulator having pulse width modulation mapping for generating a harmonic content cascaded with the digital modulator circuit, has not been shown in the prior art of record.

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Wilson et al discloses a method and apparatus for phase locking to an input signal and outputting a sigma-delta modulated control signal. The method and apparatus of the present invention provide a sigma-delta modulated control signal which can be utilized by any one of a decimator for decimating a digital data at a first data rate to a digital data at a second data rate and an interpolator for interpolating a digital data at a first data rate to a digital data at a second data rate. The decimator and the interpolator can be utilized in any one of an analog-to-digital converter, a digital-to-analog converter and a digital-to-digital converter. In one embodiment, a period of the input signal is determined and fed to a phase-locked loop which includes a sigma-delta modulator for providing the sigma-delta modulated control signal. The phase-locked loop also

includes a phase detector for determining a phase and a frequency-difference between the input signal and a conversion signal generated by the phase-locked loop. The method and apparatus thus locks to the phase and the frequency of the input signal and provide a phase-locked sigma-delta-modulated control signal.

May discloses an analog-to-digital or digital-to-analog system contains a converter (706). The converter is supplied with a clock signal (CLK1) at a frequency fs derived from a crystal of a frequency fs/N. The frequency fs is derived from the fs/N crystal frequency by using an edge-triggered clock multiplier 705 which multiplies the crystal frequency by the factor N. Sigma delta processing circuitry (702) is then used to place a null (e.g., low gain area) in the quantization noise at the same frequency where clock jitter noise is high in order to cancel the adverse cumulative effects of these two types of noise.

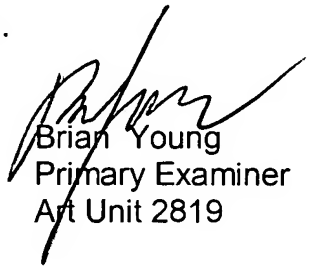
Oliver et al discloses a signal synchronization mapper for ***mapping*** an input data stream characterized by a first frequency (typically a SONET/SDH stream) into an output data stream characterized by a second frequency. A phase lock control loop containing a "delta-sigma" (.DELTA.-.SIGMA.) modulator which functions as a voltage controller oscillator synchronizes the data rate of the output stream to that of the input stream in a manner which simplifies attenuation of jitter energy when the output data stream is desynchronized (demapped). The modulator generates an accurate pulse train by duty-cycle dithered ***modulation*** of the input stream, which the mapper interprets as stuff/nullide-stuff commands such that the ***mapping*** operation is lossless over time (i.e. the number of bits in equals the number of bits out over time) thus

allowing utilization of a FIFO buffer without the need to monitor the buffer's depth or its pointers.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Young whose telephone number is 571-272-1816. The examiner can normally be reached on Mon-Fri 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Brian Young
Primary Examiner
Art Unit 2819

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